REMARKS

The Applicants respectfully request further examination and consideration in view of the above amendments and the arguments set forth fully below. Claims 1-66 were previously pending in this application. Within the Office Action, Claims 1-13 and 27-49 have been allowed, Claims 14, 19, 20, 25, 26, 50-54 and 60-66 have been rejected, and Claims 15-18, 21-24 and 55-59 have been objected to. By the above amendments, Claim 26 and 50 have been amended. Accordingly, Claims 14-26 and 50-66 are currently pending.

Explanation of changes to replacement Figures 1, 3, and 5-6

Replacement Figures 1, 3, and 5-6 now include the label --Prior Art-- next to the number of the replacement figure.

Objections to the specification

By the above amendment to Claim 50, appropriate corrections have been made to the "failure to provide proper antecedent basis for the claimed subject matter" objection specifically noted on page 3 of the Office Action.

Rejections Under 35 U.S.C. § 102

Claims 14, 19-20, 25, 50-54, 60-63 and 65 have been rejected under 35 U.S.C. 102(e) as being anticipated by Iida et al., U.S. Patent No. 6,625,713 B2 (hereinafter, "Iida"). Claims 15-18, 21-24, and 55-59 are objected to as being dependent upon a rejected base claim.

Specifically, it is stated that Iida teaches "Mapping a non volatile memory medium within the flash memory system into a plurality of independently addressable, independently programmable and independently erasable blocks (i.e., segments or blocks, e.g., cols 5-6, figs. 7, 11 and 14) including a plurality of dedicated data blocks (i.e., segments or blocks; e.g.. figs. 7A and 11A segments or fig. 7A, blocks n-1 and n; col. 5, line 55 to col. 6, line 20) and a plurality of dedicated overhead blocks comprising a first dedicated overhead block and a second dedicated overhead block (i.e., segments or blocks; e.g., figs. 7A and 11A segments or fig. 7A, blocks 0-3; fig. 7F; and col. 5, line 55 to col. 6, line 20; fig. 14C segments or block 123) . . ." The Applicants respectfully traverse this rejection.

Iida discloses a memory controller for reading data stored in a nonvolatile memory that includes a number of erasable blocks containing a number of pages. A logical/physical address

control table stored in a logical/physical address control table block of the nonvolatile memory is searched, read, and manipulated in the nonvolatile memory. [Abstract].

As shown in Fig. 7A of Iida, the storage area of the flash memory in Iida includes two boot blocks located at the head or beginning of the flash memory. The first boot block includes a header, an address indicating the position of initial bad data, and information called CIS/IDI. [col. 6, lines 39-43]. The second boot block is used as a backup area. [col. 6, lines 44-45]. The remaining blocks of the flash memory are user blocks for storing user and overhead data. As shown in Figs. 7D-7F, each user block comprises a user data area of 512 bytes and a redundant portion of 16 bytes to give a fixed size of 528 bytes. [col. 6, lines 14-16]. The redundant portion includes information such as error correction code (ECC) stored in bytes 13-15, flag data stored in the first two bytes, a management flag stored in byte 3, and logical address information in the next two bytes. **Neither Figures 7, 9, 11 or 14 nor the cited columns disclose or teach a flash memory system architecture with separate storage of overhead and user data, whereby user data and overhead data are stored in separate blocks.**

not in claims

In contrast to the teachings of Iida, the method and apparatus of the present invention segregates overhead data, such as ECC data, from user data, while maintaining a cross reference between the overhead data and the user data. A flash memory system maps a non-volatile memory medium into a plurality of independently addressable, independently programmable and independently erasable memory blocks including a plurality of dedicated data blocks and a plurality of dedicated overhead blocks. The dedicated overhead blocks comprise a first dedicated overhead block and a second dedicated overhead block. Each of the dedicated overhead blocks is mapped into a plurality of overhead pages. Each of the overhead pages is mapped into a plurality of overhead segments. The same set of segment addresses is used for each overhead page. As described above, Iida does not teach segregating overhead data from user data, which minimizes the amount of memory consumed by dedicated overhead functions and makes efficient use of overhead memory when certain logical block addresses are repeated more often than other logical block addresses. Instead, Iida discloses two boot blocks at the beginning of the flash memory to allow system initialization. The remaining blocks in Iida combine both user data and overhead data such as ECC data, flag data, and logical address data.

The independent Claim 14 is directed to a method of data storage within a flash memory including the steps of mapping a non-volatile memory medium within the flash memory system into a plurality of independently addressable, independently programmable and independently

erasable memory blocks, which includes a plurality of dedicated data blocks and a plurality of dedicated overhead blocks, the dedicated overhead blocks including a first dedicated overhead block and second dedicated overhead block, mapping each of the plurality of dedicated overhead blocks into a plurality of consecutively addressed overhead segments, wherein the plurality of segments within each dedicated overhead block are addressed according to an identical set of distinct segment addresses, each segment including a physical address register and a flag field, and correlating the first dedicated overhead block to a first group of virtual logical block addresses including a first virtual logical block address. As described above, Iida does not teach segregating overhead data from user data to minimize the amount of memory consumed by dedicated overhead functions and to make efficient use of overhead memory when certain logical block addresses are repeated more often than other logical block addresses. For at least these reasons, the independent Claim 14 is allowable over the teachings of Iida.

Claims 15-25 are dependent upon the independent Claim 14. As discussed above, the independent Claim 14 is allowable over the teachings of Iida. Accordingly, Claims 15-25 are allowable as being dependent upon an allowable base claim, and are now in condition for allowance.

The independent Claim 50 is directed to a flash memory device for storing user data including a plurality of separate, independently addressable, independently programmable and independently erasable non-volatile physical memory blocks distinguishably defined by a plurality of physical block addresses including a plurality of dedicated blocks for storing user data, and a plurality of dedicated overhead blocks for storing overhead data including a first dedicated data block and a second dedicated data block. As described above, Iida does not teach a flash memory device with separate storage of overhead and user data, whereby user data and overhead data are stored in separate blocks

Claims 51-63 and 65 are dependent upon the independent Claim 50. As discussed above, the independent Claim 50 is allowable over the teachings of Iida. Accordingly, Claims 51-63 and 65 are allowable as being dependent upon an allowable base claim, and are now in condition for allowance.

Rejection Under 35 U.S.C. § 103

Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iida as applied to claim 50 above, and further in view of applicant's admitted prior art, the current specification pages 2-12 and figs. 1-6 (hereinafter AAPA). The Applicants respectfully disagree.

Claim 64 depends from the independent Claim 50. As discussed above, Claim 50 is allowable over Iida. Accordingly, Claim 64 is also allowable as being dependent upon an allowable base claim.

Claims 26 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida as applied to claims 50 or 14 above, and further in view of Tanaka, U.S. Patent No. 6,466,177 B1 (hereinafter "Tanaka"). The Applicants respectfully disagree.

Claim 26 depends from the independent Claim 14. As discussed above, Claim 14 is allowable over Iida. Accordingly, Claim 26 is allowable as being dependent upon an allowable base claim.

Claim 66 depends from the independent Claim 50. As discussed above, Claim 50 is allowable over Iida. Accordingly, Claim 66 is allowable as being dependent upon an allowable base claim.

For the reasons given above, Applicant respectfully submit that the Claims 1-66 are in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, the Examiner is encouraged to call the undersigned at (408) 530-9700 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: 5-11-04

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CERTIFICATE OF MAILING (37 CFR§ 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

HAVERSTOCK & OWENS LLP

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